CLAIMS:

1. A semiconductor device with an integrated CMOS circuit with NMOS and PMOS transistors having semiconductor zones which are formed in a silicon substrate and which adjoin a surface thereof, which surface is provided with a layer of gate oxide on which gate electrodes are formed at those areas of the semiconductor zones which form gate zones of these transistors, such that the gate electrodes of the PMOS transistors are formed in a layer of p-type doped polycrystalline silicon and a layer of p-type doped polycrystalline silicon-germanium ($Si_{1-x}Ge_x$; $0 < x < 1$) situated between said polycrystalline silicon layer and the gate oxide, characterized in that the gate electrodes of the NMOS transistors are formed in a layer of n-type doped polycrystalline silicon without germanium.

2. A semiconductor device as claimed in claim 1, characterized in that the layer of p-type doped polycrystalline silicon-germanium ($Si_{1-x}Ge_x$) contains more than 30 at% of germanium ($x > 0.3$).

3. A semiconductor device as claimed in claim 1 or 2, characterized in that a less than 5 nm thick layer of amorphous silicon is formed between the gate oxide layer and the layer of polycrystalline silicon-germanium.

4. A semiconductor device as claimed in claim 2 or 3, characterized in that the semiconductor device comprises besides said PMOS transistors also PMOS transistors having gate electrodes which are formed in a layer of p-type doped polycrystalline silicon without germanium situated on the gate oxide, the latter PMOS transistors being equal to the former in all other respects.

5. A method of manufacturing a semiconductor device with an integrated CMOS circuit with NMOS and PMOS transistors having semiconductor zones which are formed in a silicon substrate and which adjoin a surface thereof, which surface is provided with a layer of gate oxide on which silicon-germanium gate electrodes are formed for the PMOS transistors

and silicon gate electrodes without germanium are formed for the NMOS transistors, characterized in that

the gate electrodes are formed in this method in that, in that order,

- a layer of polycrystalline silicon germanium ($Si_{1-x}Ge_x$; $0 < x < 1$) is deposited on the gate oxide layer,
- a photoresist mask is formed on the layer of polycrystalline silicon-germanium which covers said layer at the areas of PMOS transistors and does not cover it at the areas of NMOS transistors,
- an etching treatment is carried out whereby the layer of silicon-germanium is removed from the gate oxide layer at the areas of said NMOS transistors,
- the photoresist mask is removed,
- a layer of polycrystalline silicon is deposited on the structure thus formed, and
- a gate electrode is formed at the areas of said PMOS transistors in the layer of polycrystalline silicon-germanium and the covering layer of polycrystalline silicon present there, and a gate electrode is formed at the areas of said NMOS transistors in the layer of polycrystalline silicon present there.

6. A method as claimed in claim 5, characterized in that a layer of polycrystalline silicon-germanium ($Si_{1-x}Ge_x$) containing more than 30 at% of germanium ($x > 0.3$) is deposited on the gate oxide layer.

7. A method as claimed in claim 5 or 6, characterized in that first a layer of amorphous silicon less than 5 nm thick is formed on the gate oxide layer before the layer of silicon-germanium is deposited thereon.

8. A method as claimed in claim 5, 6, or 7, characterized in that gate electrodes are formed in the layer of polycrystalline silicon, in which also the gate electrodes of the NMOS transistors are formed, for the creation of PMOS transistors with silicon gate electrodes without germanium at areas reserved for these PMOS transistors.